PETTT TRAINING ANNOUNCEMENT

The DoD HPC Modernization Program (HPCMP) is pleased to announce the following training event provided by the HPCMP's Productivity Enhancement, Technology Transfer, and Training (PETTT) Program:

"Capturing and Refactoring Data Movement in Computational Kernels for Physics Simulation on Manycore Systems I"

December 6–7, 2016

HEAT Center: Aberdeen, MD

(University Center of Northeastern Maryland, 1201 Technology Drive, Aberdeen, MD)

Webcast Available

The objective of this workshop is to present performance aspects and optimizations that are related to data movement in HPC systems. The topics will range from profiling and inferring locality characteristics of an applications, to how that affects performance on current and future systems. Non-volatile memory (e.g., NVRAM) and high bandwidth memory (e.g. MCDRAM) will be discussed as representative examples.

Agenda

Tuesday, December 6

PETTT Section I: This section will discuss data movement optimizations that have been used in scientific codes, primarily to reduce the cost of transfer in memory and off-node. Examples from literature will be given to illustrate the concepts.

- 8:45 – Introduction and Motivation: Technology Landscape and Importance of Data Movement
- 9:30 – Measuring Locality with Hardware Counters (PAPI, TAU): Measuring and quantifying locality in applications using TAU as a profiling framework and PAPI to read hardware counters
- 10:00 – ADAMANT Design and Test Cases: Instrumenting and profiling applications using ADAMANT to review access patterns and profile applications data objects.

10:30 – Break

- 11:00 – Hands-on Session (TAU/ADAMANT): This hands-on session will walk through instrumentation examples, profiling applications, and using both TAU and ADAMANT.
- 11:30 – Controlling Locality and Memory Allocation (numactl, thread binding, hbw_alloc, memkind): This presentation will discuss methods and libraries to control locality by managing the allocation policies. Examples of using MCDARM on a KNL will be used to illustrate the usage of the libraries.

12:00 – Lunch

- 13:00 – Data Movement Optimizations (e.g., overlap and latency hiding, communication avoiding algorithms, software libraries): This section will discuss data movement optimizations that have been used in scientific codes, primarily to reduce the cost of transfer in memory and off-node. Examples from literature will be given to illustrate the concepts.

Industry Participation, Section II: This section focuses on current Industry insights and views for data movement.

- 14:00 – Paratools: Mini-Apps for Point/Linear solver and Jacobian as test cases for data movement for KNL

15:00 – Break

- 15:30 – Cray: Architecture and Compiler Insights on Data Movement

Wednesday, December 7

- 8:00 – INTEL: Data Movement Techniques for KNL
- 9:00 – NVIDIA/PGI: Compiler Approaches to Enhanced Data Movement / Data Movement for GPGPUs

10:00 – Break

- 10:15 – IBM: Power8/9 , CAPI, and GPGPU Architecture Influences on Data Movement and Data Structure
- 12:15 – Wrap up / Closing Comments

Instructors: Drs. Amit Majumdar, Pietro Cicotti, Mahidhar Tatineni, and Manu Shantharam (San Diego Supercomputing Center)

Technical POC: Dr. Rajiv Bendale (Rajiv.Bendale@Engilitycorp.com)

PETTT training courses are provided at no cost to users of HPCMP computer systems.
Users may review a list of available training courses with details on how to register at the HPC Centers website:
https://centers.hpc.mil/users/HPCTraining.html
For registration assistance, please contact: petttTraining@hpc.mil